REMARKS/ARGUMENTS

1. Rejection of claims 1-21 under 35 U.S.C. 112, second paragraph:

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Response:

Claims 1, 4, 7, 12, 14, and 18 have been amended to clarify the claim language. All ambiguous claim language has now been amended, and claims 1-18 should now be in condition for allowance. Claims 19-21 have been cancelled, and are no longer in need of consideration. Reconsideration of claims 1-18 is requested.

2. Rejection of claims 19-21 under 35 U.S.C. 102(b):

Claims 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (US 6,356,123).

Response:

Claims19-21 have been cancelled, and are no longer in need of consideration.

3. Introduction to new claims 22-30:

New claims 22-27 are drafted based on original claims 1-6, and contain all of the limitations from these claims except the recitation of the "(M-3)/2 serially connected first sets of clock generators". However, claim 22 does contain recitation of the "rear set circuit" which the examiner has stated is not shown in the prior art of record. Therefore claims 22-27 should be in allowable form.

New claims 28-30 are drafted to more clearly summarize the present invention method of designing a frequency divider. As shown in Figs.3 and 4, the present invention divides first and second phase shifted clocks by an odd integer value to produce first and second divided clocks. The first and second divided clocks are then fed through an XOR gate to produce the target clock with a frequency that is twice that of each of the first and second divided clocks. For making the target clock have a 50% duty cycle, the first and second phase shifted clocks are preferably 90 degrees out of phase with each other.

On the other hand, Lee et al. shows in Fig.10 that two phase shifted clocks CLK_A and CLK_B are frequency divided by a factor of six to produce divided clocks, such as clock ar and clock bf. The divided clocks then undergo an XOR operation to produce intermediate clocks having a frequency that is one-third the frequency of the phase shifted clocks.

Lee et al. does not teach dividing the phase shifted clocks by an odd integer to produce first and second divided clocks. Moreover, Lee et al. does not teach that the first and second divided clocks have a duty cycle of 50%. Therefore, claims 28-30 are patentably distinct from the teachings of the Lee et al. patent. Acceptance of new claims 22-30 is respectfully requested.

In view of the above statements in favor of patentability, the applicant respectfully requests that a timely Notice of Allowance be issued in this case

Sincerely yours,

Winston Hsu Date: August 31, 2005

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)